ABSTRACT

A resetable memory is described that includes a memory without reset capability having a data output coupled to a first input of a first multiplexer. A second input of the first multiplexer has a reset value input. A channel select for the first multiplexer is coupled to a resetable storage cell output that indicates whether a storage cell within the memory without reset capability has been written to after a reset or has not been written to after a reset.

Attorney's Docket No. 02986P013